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Description

METHOD OF MEASURING A GATE CHANNEL LENGTH OF A METAL-OXIDE SEMICONDUCTOR TRANSISTOR

BACKGROUND OF INVENTION

[0001] 1.Field of the Invention

[0002] The present invention relates to a method of measuring a gate channel length of a metal-oxide semiconductor (MOS) transistor, and more specifically, to a method of obtaining the value of an unknown gate channel length of a MOS transistor by measuring an inverse gate leakage current of a sample MOS transistor with a known gate channel length and using a predetermined equation.

[0003] 2.Description of the Prior Art

[0004] With the development of very large scale integration (VLSI), the low electricity consumption and high integration of metal-oxide-semiconductor (MOS) transistors allows them to be widely applied in the semiconductor pro-

cess. Usually, a MOS transistor comprises a gate and two semiconductor regions, called a source and drain located on each side of a capacitor with an electrical characteristic opposite to that of the silicon substrate. The major structure of the gate is composed of a gate oxide layer and a gate conductive layer. When a proper bias is added to the gate, the MOS transistor can be regarded as a solid switch to control the connection of current.

[0005] In MOS transistor fabrication, a typical method to test a MOS transistor is frequently employed to continuously test the fabricated MOS transistors in every step so as to maintain the quality of every MOS transistor. Normally several test keys distributed in a periphery region of a die that is to be tested is provided, and a testing sample MOS transistor or a testing deposition layer is simultaneously fabricated in the test key area, typically formed on a scribe line between dies, with an actual MOS transistor so that the quality of the actual MOS transistor is judged by the performance of the testing sample MOS transistor. The quality, specification and functions of the actual MOS transistor therefore are well controlled, and the yield rate of MOS transistor manufacturing is consequently improved. As the semiconductor integration processes turn

more and more complicated, it becomes one of the most important issues in the semiconductor industry to infer the characteristics of the MOS transistor correctly by measuring the value of an effective channel length of the MOS transistor precisely. Furthermore, the effective channel length of the MOS transistor is also one of the most important references for computer-aided designing (CAD).

[0006] According to the prior art, a scanning electron microscope (SEM) or a transmission electron microscopy (TEM) is frequently employed to measure the gate channel length of a MOS transistor. However, as semiconductor manufacturing technology progresses, process line width decreases to even less than 0.13 microns, so that errors often occur to the measuring results of the gate channel lengths of MOS transistors done by the SEM or TEM due to the scale limitations of the SEM and TEM. Consequently, the quality of the fabricated MOS transistors is seriously flawed, and the manufacturing yield rate is reduced as well. Therefore, it is indeed important to find out an alternative method to measure the gate channel length of a MOS transistor more precisely.

SUMMARY OF INVENTION

[0007] It is therefore a primary object of the present invention to

provide an alternative method of measuring a gate channel length of a metal-oxide semiconductor transistor (MOS transistor) so as to avoid the imprecise measuring results done by a scanning electron microscope (SEM) or a transmission electron microscopy (TEM) in the prior art.

[0008] According to the claimed invention, a surface of a silicon substrate comprises a first region within either a scribe line area or a test key area, and a second region within an active area. A first MOS transistor, comprising a first gate, and a second MOS transistor, comprising a second gate, are respectively formed in the first and second regions. A predetermined voltage is then applied respectively on the first and second MOS transistors, and a first inverse gate leakage current of the first MOS transistor and a second inverse gate leakage current of the second MOS transistor are measured thereafter. Finally, a channel length of the second gate is obtained by substituting values for the first inverse gate leakage current, the second inverse gate leakage current, channel widths of the first and the second gates, a channel length of the first gate into an predetermined equation.

[0009] It is an advantage of the present invention against the prior art that a first gate oxide layer of the first MOS tran-

sistor and a second gate oxide layer of the second MOS transistor, both having a same composition and a same uniformity, have a same thickness of less than 20 angstroms, so that a direct tunneling current density of the first gate is equal to a direct tunneling current density of the second gate as the predetermined voltage is applied to the first and second MOS transistors. Therefore, the channel length of the second gate is precisely obtained by using the predetermined equation after the first and second inverse gate leakage currents are measured. Consequently, errors of testing results of the channel length of the second gate done by a SEM or a TEM are reduced, and yield rates of subsequent processes are therefore improved as well.

[0010] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the multiple figures and drawings.

Brief Description of Drawings

[0011] Fig.1 to Fig.3 are cross-sectional views of method for measuring a gate channel length of a metal-oxide semiconductor (MOS) transistor according to the present in-

vention.

DETAILED DESCRIPTION

[0012] Please refer to Fig.1 to Fig.3 of cross-sectional views of method for measuring a gate channel length of a metal-oxide semiconductor (MOS) transistor according to the present invention. As shown in Fig.1, a surface of a silicon substrate 30 comprises a first region 32 and a second region 34. Wherein the first region 32 is within either a scribe line area or a test key area on the surface of the silicon substrate 30, and the second region 34 is within an active area on the silicon substrate 30.

[0013] *As shown in Fig.2, a first MOS transistor 36, comprising a first gate oxide layer 40 and a first gate 44 formed on the first gate oxide layer 40, and a second MOS transistor 38, comprising a second gate oxide layer 42 and a second gate 46 formed on the second gate oxide layer 40, are respectively formed within the first and second regions 32 and 34 simultaneously. Alternatively, the first and second MOS transistors 36 and 38 are orderly formed. In the embodiment of the present invention, the first and second gate oxide layers 40 and 42 have same uniformity, composition and quality. In addition, both the first and second gate oxide layers 40 and 42 have a same thickness of less than 20 angstroms. For simplicity of description, a first source (not shown) and a first drain (not shown) formed on op-*

posite sides of the first gate oxide layer 40, as well as a second source (not shown) and a second drain (not shown) formed on opposite sides of the second gate oxide layer 42, are neglected in Fig.1 to Fig.3 for those four items are not the primary subject in the present invention.

[0014] As shown in Fig.3, a predetermined voltage V is then applied respectively on the first and second gates 44 and 46, and a first inverse gate leakage current of the first gate 44 and a second inverse gate leakage current of the second gate 46 are therefore generated. Wherein when the first and second MOS transistors36 and 38 are both P-type MOS transistors, the predetermined voltage V is less than 2 volts: when the first and second MOS transistors36 and 38 are both N-type MOS transistors, the predetermined voltage V is greater than 2 volts. The first and second inverse gate leakage currents are then measured.

[0015] As described in preceding paragraphs, the first and second gate oxide layers 40 and 42 have the same thickness of less than 20 angstroms. Therefore, a direct tunneling current density of the first gate 44 is equal to a direct tunneling current density of the second gate 46 as the predetermined voltage V is applied to the first and second gates 44 and 46. Since a direct tunneling current density

is a ratio of an inverse gate leakage current to a surface area of a gate, an equation (1) is obtained as below:

[0016] $Ig_1 \div (W_1 \times L_1) = Ig_2 \div (W_2 \times L_2)$ (1)

[0017] wherein Ig_1 and Ig_2 respectively represent the first and second inverse gate leakage currents;

[0018] W_1 and W_2 respectively represent a gate channel length of the first gate 44 and a gate channel length of the second gate 46; and

[0019] L_1 and L_2 respectively respectively present a channel length of the first gate 44 and a channel length of the second gate 46.

[0020] According to the present semiconductor manufacturing processes, a gate channel width is much greater than a gate channel length, and is even much greater than the smallest division of the scale of a scanning electron microscope (SEM) or a transmission electron microscopy (TEM). In the preferred embodiment of the present invention, the channel length and width of the first gate 44 of the first MOS transistor 36, and the channel width of the second gate 46 of the second MOS transistor 38 are designed to be greater than the smallest division of the scale of a SEM or a TEM, and are therefore able to be measured. In addition, the first inverse gate leakage current of the

first gate 44 and the second inverse gate leakage current of the second gate 46 can be measured easily. Consequently, a channel length of the second gate 46 is obtained by substituting values for the first inverse gate leakage current, the second inverse gate leakage current, channel widths of the first and the second gates 44 and 46, the channel length of the first gate 44 into the equation (1). As the process line width decreases to less than 0.13 microns, the method of measuring the channel length of the second gate 46 introduced in the present invention becomes more and more important and practical.

[0021] In comparison with the prior art, the first and second gate oxide layers 40 and 42 in the present invention have same uniformity, same composition and the thickness of less than 20 angstroms, so that the direct tunneling current density of the first gate 44 is equal to the direct tunneling current density of the second gate 46 as the predetermined voltage V is applied to the first and second gates 44 and 46. Therefore, the channel length of the second gate 46 is precisely obtained by using the predetermined equation (1) after the first and second inverse gate leakage currents of the first and second gates 44 and 46 are measured. By comparing the data obtained by the equa-

tion (1) and the testing results done by a TEM or a SEM, the channel length of the second gate 46 is much precisely obtained. Consequently, errors of testing results of the channel length of the second gate 46 done by a SEM or a TEM are reduced, and yield rates of subsequent processes are therefore improved as well.

[0022] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bound of the appended claims.